Attorney Docket No.: 5580-05101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/617,080 **Confirmation No.** 3380
Applicant: Brian J. Campbell
Filed: 07/10/2003
Art Unit: 2816
Examiner: Nguyen, Linh M.
Title: Conditional Clock Buffer Circuit

MS Non-Fee Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION UNDER 37 C.F.R. § 1.131

Sir:

As part of the response to the Office Action mailed December 17, 2003, please enter the attached declaration of Brian J. Campbell.

Applicant submits that this application is a continuation application of application number 10/127,103, filed April 22, 2002. The same Weiss reference was cited in that parent case in rejecting the claims of the parent application. Brian J. Campbell submitted a declaration under 37 C.F.R. § 1.131 to antedate Weiss. Accordingly, a copy of the Campbell declaration is being submitted herein in response to the rejection based on the Weiss reference to also antedate Weiss in this continuation case. Applicant requests the Examiner to enter the declaration for this continuation case as well.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/127,103
Filed: April 22, 2002
Inventor(s):
Brian J. Campbell

Title: Conditional Clock Buffer Circuit

Examiner: Nguyen, Linh M.
Group/Art Unit: 2816
Atty. Dkt. No: 5580-05100

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Lawrence J. Merkel
Printed Name

Signature 3/3/03
Date

DECLARATION UNDER 37 C.F.R. § 1.131 OF INVENTION OF BRIAN J. CAMPBELL

I, Brian J. Campbell, do hereby declare as follows:

1. I am the inventor of the subject matter of the above-styled patent application.

Conception

2. Before February 4, 2002 and within the United States, I conceived of a conditional clock buffer circuit (the "Circuit").

3. Attached hereto as Exhibit A is a circuit schematic of one embodiment of the Circuit. Attached hereto as Exhibit B is an email containing a copy of the computer file date of the schematic file containing the circuit schematic of Exhibit A. The computer date has been redacted, but is prior to February 4, 2002.

4. Attached hereto as Exhibit C is a copy of a hand-drawn schematic of one embodiment of the Circuit. The schematic bears a date prior to February 4, 2002 (actual date redacted). Additionally, the schematic is witnessed on February 5, 2002.

5. Prior to February 4, 2002, I described the Circuit to Sribalan Santhanam. A copy of a Declaration by Mr. Santhanam is attached as Exhibit D.

Diligence

6. Before February 4, 2002 and through at least April 22, 2002, I was working full-time for Broadcom Corporation, including working on a project for which I designed the Circuit. I also diligently worked toward filing a patent application for the Circuit during the above time period. I disclosed the Circuit to Broadcom Corporation's legal department, who assigned Lawrence J. Merkel (a patent agent) to prepare a patent application for the Circuit. Mr. Merkel and I met on February 26, 2002 to discuss the Circuit.

7. Between February 26, 2002 and April 2, 2002, Mr. Merkel prepared a patent application for the Circuit. Mr. Merkel mailed the first draft of the application to me on April 2, 2002. Attached as Exhibit E is a copy of a letter dated April 2, 2002 from Mr. Merkel to me, providing me with the first draft of the application.

8. Between April 2, 2002 and April 12, 2002, I received the first draft of the application, reviewed the application, and provided review comments to Mr. Merkel. On April 12, 2002, Mr. Merkel mailed me a final draft of the application. Attached as Exhibit F is a copy of a letter dated April 12, 2002 from Mr. Merkel to me, providing me with the final draft of the application along with the declaration and assignment forms for my execution.

9. Between April 12, 2002 and April 16, 2002, I received the final draft, reviewed the final draft, and executed the declaration and assignment. As noted on the declaration and assignment in the captioned application, I signed the declaration and

assignment on April 16, 2002. I returned the documents to Mr. Merkel, who filed the application in the United States Patent and Trademark Office on April 22, 2002.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application of any patent issued thereon.

Name: Brian J. Campbell

Signature: Brian J. Campbell

Date: 2/26/03

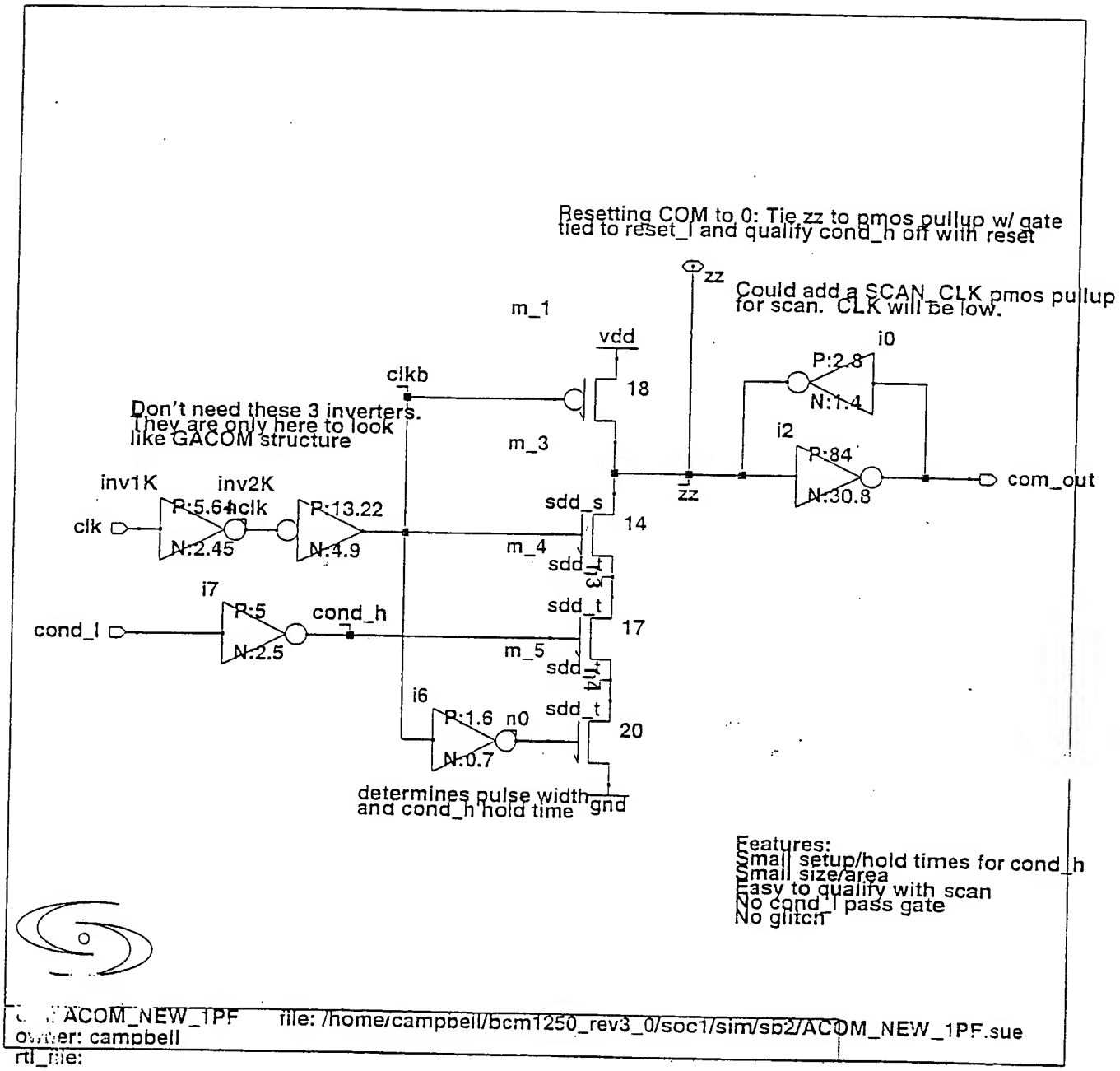

Resetting COM to 0: Tie zz to pmos pullup w/ gate tied to reset_l and qualify cond_h off with reset
zz
Could add a SCAN_CLK pmos pullup for scan. CLK will be low.
m_1
vdd
i0
P:2.8
N:1.4
clkb
18
Don't need these 3 inverters. They are only here to look like GACOM structure
m_3
i2
P:84
N:30.8
com_out
inv1K
inv2K
P:5.64
P:13.22
clk
nclk
N:2.45
N:4.9
sdd_s
14
m_4
sdd
i13
i7
P:5
cond_h
sdd_t
17
cond_l
N:2.5
m_5
sdd
i14
i6
P:1.6
n0
sdd_t
20
N:0.7
determines pulse width and cond_h hold time
gnd
Features:
Small setup/hold times for cond_h
Small size/area
Easy to qualify with scan
No cond_l pass gate
No glitch
ACOM_NEW_1PF
file: /home/campbell/bcm1250_rev3_0/soc1/sim/sb2/ACOM_NEW_1PF.sue
owner: campbell
rtl_file:

Exhibit A

y Merkel

rom: Brian Campbell [campbell@broadcom.com]
Sent: Tuesday, February 26, 2002 8:06 PM
To: Larry Merkel
Subject: Clock Buffer schematic file date

Larry,

Here is a cut-n-paste of my clock buffer schematic file date:

ll /home/campbell/bcm1250_rev3_0/soc1/sim/sb2/ACOM_NEW_1PF.sue
-rw-rw-r-- 1 campbell users 4394 . 18:04 /home/campbell/bcm1250_rev3_0/soc1/sim/sb2/ACOM_NEW_1PF.sue

Thanks,
Brian

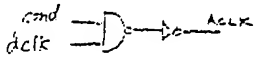
--
Brian Campbell
Broadcom Corporation
campbell@broadcom.com
(408) 922-7067

Exhibit B

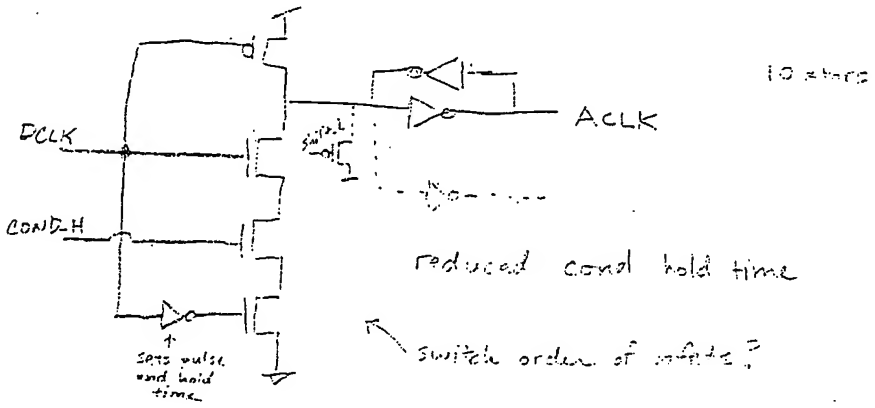
532

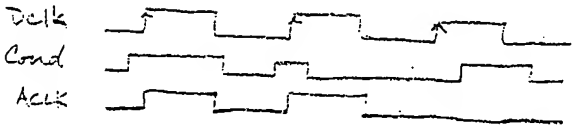
Scan

Conn (New Design)



Ⓐ





Witnessed and Understood by: 2/5/2002

Exhibit C

Declaration

1. Prior to February 4, 2002, Brian J. Campbell described a conditional clock buffer circuit to me. The clock buffer circuit is illustrated in Fig. 1 attached hereto. References to transistors and nodes below refer to labels on Fig. 1.

2. Prior to February 4, 2002, Mr. Campbell explained that the transistor T2 and the transistor T4 would be used to create a window of time, from the rising edge of Clk to a falling edge on the node N1 caused by the rising edge, in which the condition signal Con on the gate of the transistor T3 can cause the discharge of the internal node N2 (and thus the transition high of the output O).

3. Prior to February 4, 2002, Mr. Campbell explained that the width of the window of time would be controlled by the delay in the inverter whose output is connected to the node N1.

4. Prior to February 4, 2002, Mr. Campbell explained that the circuit would provide a small setup time for the condition signal Con (with respect to the rising edge of Clk).

5. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Sribalan Santhanam

5/24/02
Date

Exhibit D Page 1

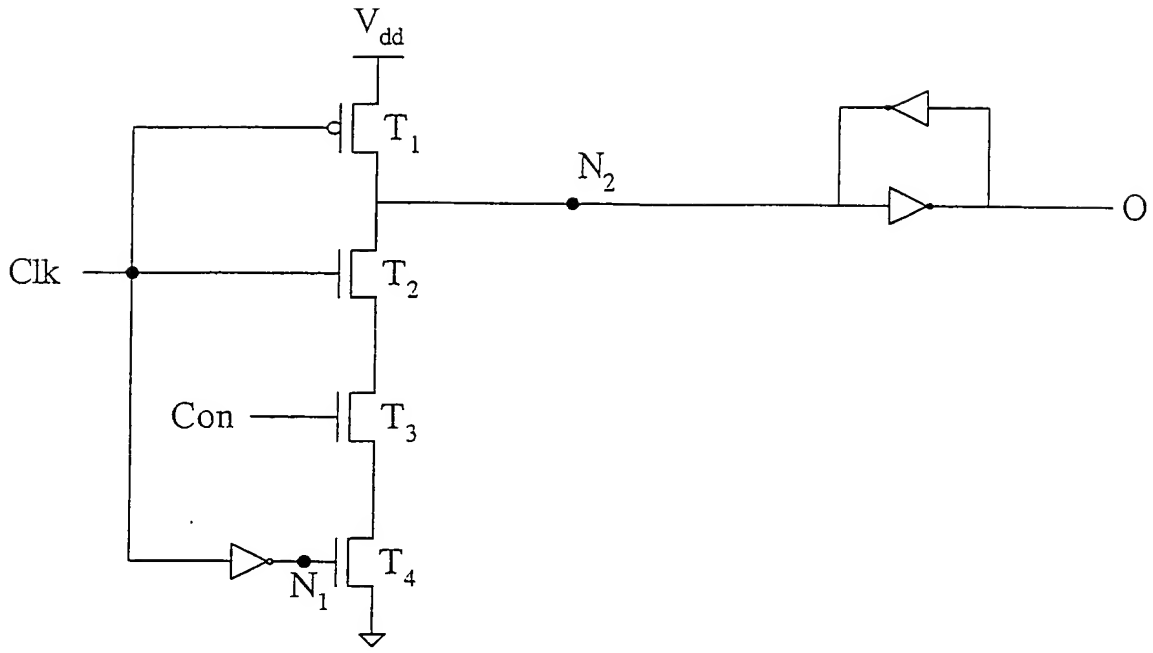


Fig. 1

Exhibit D, Page 2

INTELLECTUAL PROPERTY LAW
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COPYRIGHTS AND
UNFAIR COMPETITION

CONLEY, ROSE & TAYON
A PROFESSIONAL CORPORATION
THE CHASE BUILDING
700 LAVACA, SUITE 800
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FACSIMILE (512) 703-1250
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CHASE TOWER
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HOUSTON, TEXAS 77002-2912
(713) 238-8000
FACSIMILE (713) 238-8008

Lawrence J. Merkel
Patent Agent
(512)703-1253

5580-05100
BP2230

April 2, 2002

Brian J. Campbell
Broadcom Corporation
2451 Mission College Blvd.
Santa Clara, CA 95054

RE: U.S. Patent Application Entitled: "**CONDITIONAL CLOCK BUFFER CIRCUIT**" -- *Brian J. Campbell* (Our Ref: 5580-05100; Your Ref: BP2230)

Dear Brian:

Enclosed is a first draft of the above-referenced patent application. Please review the attached application carefully to ensure that all aspects of the invention are included and further to ensure that your invention is properly and completely described. Also, please see the enclosed memo pertaining to the Duty of Disclosure.

I look forward to making any changes to this draft application in preparation for filing the final draft application and supporting papers with the U.S. Patent and Trademark Office.

If you have any questions, please do not hesitate to call me at (512)703-1253.

Very truly yours,

Lawrence J. Merkel

LJM:dmp
Enclosures

Exhibit E

K:\BM\Broadcom\05100\Ltr\Firstdraft.051.Doc

INTELLECTUAL PROPERTY LAW
INCLUDING
PATENTS, TRADEMARKS,
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Lawrence J. Merkel
Patent Agent
(512)703-1253

5580-05100
BP2230

April 12, 2002

Brian J. Campbell
Broadcom Corporation
2451 Mission College Blvd.
Santa Clara, CA 95054

RE: U.S. Patent Application Entitled: "CONDITIONAL CLOCK BUFFER CIRCUIT" -- *Brian J. Campbell* (Our Ref: 5580-05100; Your Ref: BP2230)

Dear Brian:

Enclosed is the above-referenced patent application, including a Declaration/Power of Attorney form and an Assignment. Please sign and date all forms and have a witness sign and date the Assignment. Return all executed forms to me for filing with the U.S. Patent and Trademark Office.

If you have any questions, please do not hesitate to call me at (512)703-1253.

Very truly yours,

Lawrence J. Merkel

LJM:dmp
Enclosures

Cc: Angel Atondo (with enclosures)
Dee Henderson (with enclosures)

K:\B\Broadcom\05100\Ltr\Finaldrft.051.Doc

Exhibit F